Claims

[c1] 1. A mask read-only-memory (ROM) structure, comprising:
a substrate;
a buried bit line embedded inside the substrate;
a patterned stack layer covering a portion of the upper surface of the substrate, wherein the stack layer comprises a first dielectric layer, a stopping layer and a second dielectric layer;
a gate oxide layer covering a portion of the upper surface of the substrate; and
a word line crossing over the buried bit line to form a plurality of coding cells, wherein the coding cells having a stack layer thereon are at a first data state while the coding cells having a gate oxide layer thereon are at a second data state.

[c2] 2. The mask ROM of claim 1, wherein the stack layer includes a first silicon oxide layer, a silicon oxynitride layer and a second silicon oxide layer stacked on top of each other.

[c3] 3. The mask ROM of claim 1, wherein the stack layer includes a first silicon oxide layer, a silicon nitride layer

and a second silicon oxide layer stacked on top of each other.

[c4] 4. The mask ROM of claim 1, wherein the first dielectric layer has a thickness between about 200Å to 800Å.

[c5] 5. The mask ROM of claim 1, wherein the stopping layer has a thickness between about 20Å to 80Å.

[c6] 6. The mask ROM of claim 1, wherein the second dielectric layer has a thickness between about 200Å to 800Å.